What is claimed is:

1. A semiconductor memory device including word lines provided for every row of a memory cell and bit lines provided for every column of the memory cell, wherein a memory cell array is configured by arranging in a matrix memory cells for storing data in accordance with stored charges of capacity elements, comprising:

a write gate provided between a bit line and an input/output data line, which becomes a conductive state when a selected word line becomes an activation state when writing and selectively applies to the bit line a write signal applied to an input output data line in accordance with write data.

2. A semiconductor memory device as set forth in claim 1, comprising a decoder circuit wherein said write gate comprises a switching element connected between the bit line and input/output data line, and generates a selection signal for making the switching element corresponding to a column selected by an input address conductive and supplies to the write gate when writing.

3. A semiconductor memory device as set forth in claim 1, wherein a bit line pair composed of two bit

lines is provided to each column and two bit lines of the bit pair are arranged to be a twist layout in the memory cell array.

4. A semiconductor memory device including word lines provided for every row of a memory cell and bit lines provided for every column of the memory cell, wherein a memory cell array is configured by arranging in a matrix memory cells for storing data in accordance with stored charges of capacity elements, comprising:

a column selection circuit for selecting one from a plurality of column in accordance with an address; and

a write gate provided between the column selection circuit and input/output data line, which becomes a conductive state when a selected word line becomes an activation state when writing and applies to the selected bit line a write signal applied to the input/output data line in accordance with write data via the column selection circuit.

5. A semiconductor memory device as set forth in claim 4, wherein a bit line pair composed of two bit lines is provided to each column and two bit lines of the bit pair are arranged to be a twist layout in the memory

cell array.

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